AMENDMENTS TO THE CLAIMS

Please cancel Claims 5, 10, 15 and 23-24. Please accept amended Claims 1-4, 6, 8, 9, 11 and 13 as follows:

1. (Currently Amended) A system of cache residence prediction in a computer system, comprising:

a plurality of caches, comprising a first cache and one or more other caches; and

a prediction mechanism predicting that data requested by the first cache of a cache miss can be found in at least one of the one or more other caches, if an address of the cache miss matches an address tag of a cache line in the first cache and the cache line in the first cache is in an invalid state, wherein the prediction mechanism further comprises a prediction table, wherein each entry in the prediction table corresponds to one or more cache lines determined by a hash function.

2. (Currently Amended) The system of claim 1, wherein the ~~prediction mechanism further comprises a~~ prediction table ~~that~~ records one or more addresses of one or more recently replaced invalid cache lines.

3. (Currently Amended) The system of claim 1, wherein the ~~prediction mechanism further comprises a~~ prediction table ~~that~~ records one or more addresses of one or more recently replaced shared cache lines.

4. (Currently Amended) The system of claim 1, wherein the ~~prediction mechanism further comprises a~~ prediction table ~~that~~ records prediction information for one or more super-blocks,

wherein each of the one or more super-blocks comprises one or more cache lines, and wherein each entry in the prediction table includes a super-block address and a valid vector that has a valid bit for each of the one or more cache lines.

5. (Cancelled)

6. (Currently Amended) A system of cache residence prediction in a computer system, comprising:

a plurality of caches, comprising a first cache and one or more other caches;

a memory and a memory controller operatively coupled to the memory; and

a prediction mechanism operatively coupled to the first cache, the prediction mechanism predicting whether data requested by the first cache of a cache miss can be supplied by at least one of the one or more other caches, producing a prediction result, and sending the prediction result to the memory controller; wherein the memory controller uses the prediction result to determine if the memory is to be accessed immediately, or if the memory is not to be accessed until a corresponding cache snoop operation shows that the data requested by the first cache cannot be supplied by at least one of the one or more other caches, wherein the prediction mechanism further comprises a prediction table that records prediction information for one or more super-blocks, wherein each of the one or more super-blocks comprises one or more cache lines, and wherein each entry in the prediction table includes a super-block address and a valid vector that has a valid bit for each of the one or more cache lines..

7. (Original) The system of claim 6, wherein the prediction mechanism predicts that the data requested by the first cache of a cache miss can be supplied by at least one of the one or more other caches, if the address of the cache miss matches an address tag of a cache line and the cache line is in an invalid state.

8. (Currently Amended) The system of claim 6, wherein the ~~prediction mechanism further comprises a~~ prediction table ~~that~~ records one or more addresses of one or more recently replaced invalid cache lines.

9. (Currently Amended) The system of claim 6, wherein the ~~prediction mechanism further comprises a~~ prediction table ~~that~~ records one or more addresses of one or more recently replaced shared cache lines.

10. (Cancelled)

11. (Currently Amended) The system of claim 6, wherein ~~the prediction mechanism further comprises a prediction table, wherein~~ each entry in the prediction table corresponds to one or more cache lines determined by a hash function.

12. (Original) The system of claim 6, wherein the memory can be a cache and the memory controller can be a cache controller of the cache.

13. (Currently Amended) A system of memory residence prediction in a computer system, comprising:

a plurality of caches, comprising a first cache and one or more other caches;

a memory and a memory controller operatively coupled to the memory; and

a prediction mechanism predicting whether data requested by the first cache of a cache miss can be found in at least one of the one or more other caches, and producing a prediction result; wherein the prediction mechanism comprises a prediction table that is updated accordingly when the prediction mechanism observes a cache operation that can affect whether data requested by the first cache of a future cache miss can be found in at least one of the one or more other caches, wherein the prediction mechanism removes an address from the prediction table, if the memory controller observes a cache operation indicating that requested data by the first cache of a future cache miss on the address cannot be found in at least one of the one or more other caches.

14. (Original) The system of claim 13, wherein the prediction mechanism records an address in the prediction table, if the prediction mechanism observes a cache operation indicating that requested data by the first cache of a future cache miss on the address can be found in at least one of the one or more other caches.

15. (Cancelled)

16. (Original) The system of claim 13, wherein the memory controller uses the prediction result to determine if the memory is to be accessed immediately, or if the memory is not to be accessed

until a corresponding cache snoop operation shows that the requested data cannot be supplied by at least one of the one or more other caches.

17. (Original) The system of claim 13, wherein the prediction table records prediction information for one or more super-blocks, wherein each of the one or more super-blocks contains one or more cache lines, and wherein each entry in the prediction table further comprises a valid vector that has a valid bit for each of the one or more cache lines.

18. (Original) The system of claim 13, wherein each table entry of the prediction table corresponds to one or more cache lines determined by a hash function.

19. (Original) The system of claim 13, wherein the memory can be a high-level cache and the memory controller can be a cache controller of the cache.

20. (Original) A system of memory residence prediction in a computer system, comprising:

a plurality of caches, comprising a first cache and one or more other caches;

a memory and a memory controller operatively coupled to the memory, a first prediction mechanism operatively coupled to the first cache, the first prediction mechanism predicting whether data requested by the first cache of a cache miss can be supplied by at least one of the one or more other caches, producing a first prediction result, and sending the first prediction result to the memory controller; and

a second prediction mechanism operatively coupled to the memory, the second prediction mechanism predicting whether requested data by the first cache of a cache miss can be supplied

by at least one of the one or more other caches, and producing a second prediction result; wherein an overall prediction result is determined by the first prediction result and the second prediction result; and

wherein the memory controller uses the overall prediction result to determine if the memory is to be accessed immediately, or if the memory is not to be accessed until a corresponding cache snoop operation shows that the data requested by the first cache cannot be supplied by at least one of the one of more other caches.

21. (Original) The system of claim 20, wherein the overall prediction result comprises predicting that data requested by the first cache can be supplied by at least one of the one or more caches, if the first prediction result or the second prediction result predicts that the data requested by the first cache can be supplied by at least one of the one or more caches.

22. (Original) The system of claim 20, wherein the memory can be a high-level cache and the memory controller can be a cache controller of the cache.

23-24. (Cancelled)